REMARKS

Claims 1, 8, 10, 12, 17, 19, 20, 22, 23, 30, 32, 33, 35, 36, 38, 39, 41 and 42 have been amended. Claims 11, 15, 16, 18, 24-29, 31 and 37 have been canceled. The application contains claims 1-10, 12-14, 17, 19-23, 30, 32-36 and 38-42. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications.

Claims 1-42 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite. The rejection is respectfully traversed. The Office Action lists several concerns, which are not listed here for convenience purposes. Applicant respectfully submits, however, that claims 1, 8, 10, 12, 17, 19, 20, 22, 23, 30, 32, 33, 35, 36, 38, 39, 41 and 42 have been amended and other claims canceled to address the concerns raised in the Office Action. Accordingly, remaining claims 1-10, 12-14, 17, 19-23, 30, 32-36 and 38-42 are in compliance with 35 U.S.C. §112. Applicant respectfully submits that the rejection should be withdrawn and claims 1-10, 12-14, 17, 19-23, 30, 32-36 and 38-42 allowed.

Claims 1-42 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Ichiriu. The rejection is respectfully traversed.

Claim 1 recites a method for testing a memory device. The method comprises the steps of "enabling output from a match line under test; decoding an address of a selected memory storage location corresponding to said match line under test; loading said selected memory storage location and a comparand register with a known data pattern; performing a search operation, for the known data pattern in the comparand register, on said memory device; outputting a result of said search operation; comparing said result of said search operation with an expected result of said search operation, said expected result comprising an expected match indication on

the match line under test; confirming proper operation of said memory device if said result of said search operation is equal to said expected result of said search operation; and indicating an error of said memory device if said result of said search operation is not equal to said expected result of said search operation." Applicant respectfully submits that Ichiriu fails to disclose, teach or suggest the claimed invention.

Ichiriu, by contrast, discloses testing for parity errors of CAM cells and error correction when errors are found. There is no disclosure anywhere in Ichiriu for testing physical match lines for errors. That is, Ichiriu never has a "match line under test" because Ichiriu is only concerned with performing "simultaneous write and compare" functions and performing parity testing and error correction on the CAM cells themselves. There is no testing of match lines in Ichiriu. Absent this teaching, Ichiriu must fail to disclose, teach or suggest the acts of (or circuitry for) "enabling output from a match line under test; decoding an address of a selected memory storage location corresponding to said match line under test; loading said selected memory storage location and a comparand register with a known data pattern; performing a search operation, for the known data pattern in the comparand register, on said memory device; outputting a result of said search operation; comparing said result of said search operation with an expected result of said search operation, said expected result comprising an expected match indication on the match line under test; confirming proper operation of said memory device if said result of said search operation is equal to said expected result of said search operation; and indicating an error of said memory device if said result of said search operation is not equal to said expected result of said search operation." These steps are simply not found in Ichiriu.

Accordingly, claim 1 is allowable over Ichiriu. Claims 2-7 depend from claim 1 and are allowable along with claim 1.

Claim 8 recites "enabling said match line of a set of memory cells being tested and disabling match lines of other sets of memory cells; storing items of data matching the data item stored in the comparand register in the set of memory cells being tested; and receiving output signals from said match lines and determining whether said output signals indicate that said set of memory cells being tested has items of stored data that match the data item stored in a comparand register." Accordingly, for at least the reasons set forth above, claim 8 is allowable over Ichiriu. Claims 9 and 10 depend from claim 8 and are allowable along with claim 8.

Claim 12 recites "a circuit coupled to said match line under test, said corresponding word line, and a test mode match line reset signal, said circuit determining a status of the match line under test based on a result of a search operation and a signal on the match line under test." Accordingly, for at least the reasons set forth above, claim 12 is allowable over Ichiriu. Claims 13 and 14 depend from claim 12 and are allowable along with claim 12.

Claim 17 recites "comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register; and enabling circuitry that enables a match line to provide said match signal as an output when said set of memory cells is being tested." Accordingly, for at least the reasons set forth above, claim 17 is allowable over Ichiriu. Claim 19 depends from claim 17 and is allowable along with claim 17.

Claim 20 recites "comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register." Accordingly, for at least the reasons set forth above, claim 20

is allowable over Ichiriu. Claims 21 and 22 depend from claim 20 and are allowable along with claim 20.

Claim 23 recites a "circuit coupled to said match line under test, said corresponding word line, and a test mode match line reset signal, said circuit determining a status of the match line under test based on a result of a search operation and a signal on the match line under test." Accordingly, for at least the reasons set forth above, claim 23 is allowable.

Claim 30 recites "comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register." Accordingly, for at least the reasons set forth above, claim 30 is allowable over Ichiriu. Claim 32 depends from claim 30 and is allowable along with claim 30.

Claim 33 recites "comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register." Accordingly, for at least the reasons set forth above, claim 33 is allowable over Ichiriu. Claims 34 and 35 depend from claim 33 and are allowable along with claim 33.

Claim 36 recites "comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register." Accordingly, for at least the reasons set forth above, claim 36

is allowable over Ichiriu. Claims 38, 40 and 41 depend from claim 36 and are allowable along with claim 36.

Claim 39 recites "comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register." Accordingly, for at least the reasons set forth above, claim 39 is allowable.

Claim 42 recites "loading said selected memory storage location with a known data pattern; loading a comparand register with said known data pattern; performing a search operation, for the known data pattern in the comparand register, on said memory device; and outputting a result of said search operation; comparing said result of said search operation with an expected result of said search operation, said expected result comprising an expected match indication on the match line under test; confirming proper operation of said memory device if said result of said search operation is equal to said expected result of said search operation; and indicating an error of said memory device if said result of said search operation is not equal to said expected result of said search operation." Accordingly, for at least the reasons set forth above, claim 42 is allowable.

Applicant respectfully submits that the rejection should be withdrawn and claims 1-10, 12-14, 17, 19-23, 30, 32-36 and 38-42 allowed.

Moreover, Applicant notes that the Office Action indicates that claims 30-35 are substantial duplicates of claim 17-22. Applicant respectfully traverses this statement. Claims 30-35 recite an "integrated circuit" while claims 17-22 recite a "memory circuit." An integrated circuit has a known meaning in the art and is

different from a memory circuit, which may or may not be an integrated circuit. Moreover, claims 18 and 31 have been canceled. Thus, claims 30 and 32-35 are not substantial duplicates of claims 17 and 19-22.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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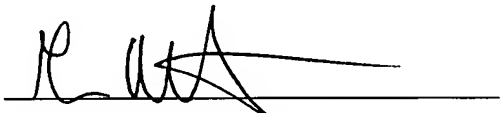
Respectfully submitted,



Thomas J. D'Amico
Registration No.: 28,371
Gianni Minutoli
Registration No.: 41,198
DICKSTEIN SHAPIRO MORIN &
OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant